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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/690,200	10/21/2003	Salman Akram	4244.5US (97-1355.05/US)	3680
24247	7590	07/27/2006	EXAMINER	
TRASK BRITT P.O. BOX 2550 SALT LAKE CITY, UT 84110			DOLAN, JENNIFER M	
			ART UNIT	PAPER NUMBER
			2813	

DATE MAILED: 07/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/690,200

Applicant(s)

AKRAM ET AL.

Examiner

Jennifer M. Dolan

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 May 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 6-10 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 6-10 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 2 May 2006 has been entered.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 6-10 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claims contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention.

Claim 6 requires a gate structure having a gate oxide layer formed on the dielectric layer, an adhesion layer formed on the gate oxide layer and a metal silicide layer formed on the adhesion layer, the gate structure having a first sidewall and a second sidewall. The specification does not provide any disclosure or even a suggestion of a gate stack of this nature, but rather, the specification clearly indicates that the gate structure is a polysilicon-metal-dielectric stack (i.e.

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polysilicon disposed on the gate dielectric layer, metal silicide on the polysilicon, and a dielectric capping layer on the silicide layer; see paragraphs 0028-0033). It is not clear whether the Applicant intends to claim a multilayer gate dielectric layer, such as the ONO layer in paragraph 0027 (thus making the “gate oxide layer” part of the blanket deposited dielectric layer and not part of the gate structure having sidewalls), whether the Applicant intends to claim the additional protective oxide layers as in paragraph 0034 (which are clearly disclosed as being formed over the areas through which introduction of dopants occurs – i.e., the areas *not* under the gate – thus making such layers not part of the gate structure having sidewalls), or whether the Applicant intends to simply claim that the gate structure includes the polysilicon-metal silicide-dielectric structure as described in the specification.

For the purpose of examination, it is assumed that the gate structure includes the polysilicon-metal silicide-dielectric structure corresponding to the specification.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 6-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,866,460 to Akram et al. (cited by Applicant) in view of U.S. Patent No. 5,739,066 to Pan.

Akram discloses a method of making a transistor on a substrate (10) having a dielectric layer (14) thereon comprising: forming a gate structure (20,22,24; see figures 2A, 3A) overlying

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the dielectric layer, the gate structure including a polysilicon (20)-metal silicide (22)-dielectric (24) stack, the gate structure having first and second sidewalls (see figure 3A), defining a first contact region (region to the left of gate structure including regions 16,40, and 34), a second contact region (region to the right of gate structure including regions 16,40,34) and a channel region therebetween; and forming first (16), second (40), and third (34) subregions within the contact regions (see figures 3A-3C), each subregion having a different doping concentration from the other subregions (see column 6, lines 17-35), wherein forming the subregions comprises the steps of: introducing a first dopant into the substrate to form the first subregion (16), the first subregion generally aligned with the sidewalls of the gate structure (figure 3A; column 7, lines 40-45); forming a single layer sidewall spacer (26) overlying the sidewalls, the single layer sidewall spacer having a relatively large thickness of 150-2000 angstroms (column 5, line 60-column 6, line 10); introducing a second dopant into the substrate to form the second subregion (40), the second subregion generally aligned with the second single layer sidewall spacer (figure 3B); reducing the thickness of the single layer sidewall spacer to form a sidewall spacer having a thickness reduced from that of the single layer sidewall spacer (see column 7, lines 20-35; figure 3C); and introducing a third dopant into the substrate to form the third subregion (34), the third subregion generally aligned with the third sidewall spacer (figure 3C).

Akram fails to teach formation of the first single layer sidewall spacer of a thin conformal layer of dielectric material.

Pan teaches that it is advantageous when forming a stacked gate structure substantially similar to that in Akram (see Pan, column 3, lines 1-20; figures 1-4) to include a first thin layer sidewall spacer (34,36) formed of silicon nitride (column 3, lines 20-27) overlying the gate

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sidewalls (figure 3), the first single thin layer sidewall spacer being formed by depositing a thin conformal layer of dielectric material (32) over the substrate (figure 2) and etching to a predetermined thickness over the sidewalls (column 3, lines 20-40; column 4, lines 39-40; note that the post-etched thickness must be less than the deposited thickness of 50-500 angstroms); and providing an annealing/oxidation step at an elevated temperature (column 3, lines 40-67). The first thin layer sidewall spacer is disposed underneath additional sidewall spacer layers (see figures 5 and 7).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the thin conformal sidewall spacer and methods of forming such a layer, as taught by Pan, in the transistor formation method of Akram. The rationale is as follows: A person having ordinary skill in the art would have been motivated to include the conformal spacer underlying the additional spacers of Akram, because Pan illustrates that formation of a thin sidewall spacer followed by an annealing/oxidation step helps repair damage to the gate dielectric layer resulting from the gate stack etching and helps oxidize the portions of the polysilicon gate layer interfacing the gate dielectric layer, thus reducing hot electron degradation (see Pan, column 1, lines 25-45; column 3, line 40 – column 4, line 10). The Examiner notes that since the first sidewall spacer is disclosed as preferably 100 angstroms and as low as 50 angstroms, it is expected to be etched to a thickness between 50-150 angstroms (Pan, column 3, lines 20-40; column 4, lines 39-40), and since the second spacer is disclosed as 150-2000 angstroms, thus overlapping the claimed 550 angstroms (Akram, column 5, line 60-column 6, line 10), these conditions are generally consistent with the claimed 2 to 20 times the thickness of the first layer. Although neither Akram nor Pan provides an exact value for the spacer thicknesses, it

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has been held that “where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.” In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (1955).

Response to Arguments

6. Applicant's arguments with respect to claims 6-10 have been considered but are generally moot in view of the new grounds of rejection.

The Applicant argues that the gate structure including a gate oxide layer on the dielectric layer and a metal silicide on the gate oxide layer are disclosed in paragraphs 0028-0030. The Applicant further states that the “gate oxide layer” is one of the “additional oxide layers” appearing in paragraph 0034.

The Examiner disagrees with this characterization. Paragraphs 0028-0030 clearly indicate that the gate structure is a polysilicon-metal silicide-dielectric stack. There is no mention of an oxide layer disposed in the gate structure and on top of the gate dielectric layer. In paragraph 0034, the “additional oxide layers” are clearly disclosed as being deposited “to increase the thickness of the gate dielectric 14 *in areas where process steps, e.g., the introduction of dopants, are to be performed.*” Hence, these additional oxide layers are disposed upon the gate dielectric layer outside of the gate stack, (i.e., in regions overlying dopant regions 16-18), and hence, are not part of the gate structure having sidewalls. It would be unexpected and generally disadvantageous in the MOSFET arts to dispose additional oxide layers upon the

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gate dielectric within the gate stack, since doing so would effectively increase the thickness of the gate dielectric.

Regarding the assertion that Akram does not disclose a gate oxide on a gate dielectric layer, the Examiner respectfully points out that the Akram '460 reference includes the same clause about additional oxide layers being optionally present in the regions where implantation is to occur (see Akram, column 4, line 60 – column 5, line 5) that the Applicant appears to be relying on to show written description of the gate oxide layer. Hence, if the “gate oxide layer” is included in the present application, it is also included in the Akram '460 reference.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Dolan whose telephone number is (571) 272-1690. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jennifer M. Dolan
Examiner
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jmd


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